WHAT IS CLAIMED IS:

1. A macro cell for an integrated circuit design having an input-output (IO) region with a plurality of IO buffer cells physically dispersed with other cells in IO slots along an interface portion of the IO region, the macro cell comprising:

a plurality of macro cell IO signal slots that are physically dispersed so as to substantially align with the IO buffer cells in the interface portion; and

an interface definition comprising a plurality of source-synchronous interface IO signal nets including a multiple-bit data bus and a first clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the first clock strobe net, wherein the nets are routed to corresponding ones of the plurality of macro cell signal slots, and wherein the macro cell is adapted to be instantiated as a unit in the integrated circuit design.

2. The macro cell of claim 1 wherein the macro cell IO signal slots are dispersed among other, unused IO slots within the macro cell.

3. The macro cell of claim 1 wherein:

the plurality of interface IO signal nets further comprises a second clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the first and second clock strobe nets.

4. The macro cell of claim 3 wherein the interface definition defines circuitry adapted to transfer data over the data bus at a first data rate with every other transition on at least one of the first and second clock strobe nets and at a second, faster data rate with each transition on at least one of the first and second clock strobe nets.

5. The macro cell of claim 3 wherein:

each bit of the multiple-bit data bus comprises a transmit bit, a receive bit and an enable bit; and

the respective macro cell IO signal slot for each of bit of the data bus defines physical pin locations for the transmit bit, receive bit and enable bit.

6. The macro cell of claim 1 wherein the interface definition defines a transceiver configured to implement a PCI-X 2.0 physical layer interface specification.

7. The macro cell of claim 1 wherein the plurality of IO buffer cells is physically dispersed with other cells selected from the group comprising decoupling capacitor cells, electrostatic discharge protection cells and power supply cells.

8. A macro cell for instantiation in an integrated circuit design, the macro cell comprising:

a physical layer interface definition comprising a multiple-bit data bus and a first clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the clock strobe net; and

a plurality of macro cell input-output (IO) slots, which are electrically coupled to respective bits in the multiple-bit data bus and the first clock strobe net and are physically dispersed from one another in a spacing pattern that is defined for at least one integrated circuit package type, wherein the macro cell is adapted to be instantiated in the integrated circuit design as a unit.

9. The macro cell of claim 8 wherein:

the spacing pattern is defined for a plurality of different integrated circuit package types.

10. The macro cell of claim 8 wherein:

the integrated circuit design has an IO region with a plurality of IO buffer cells physically dispersed with other cells in IO slots along an interface portion of the IO region according to the package type; and

the plurality of macro cell IO signal slots are physically dispersed so as to substantially align with corresponding ones of the IO buffer cells along the interface portion.

11. The macro cell of claim 10 wherein the plurality of IO buffer cells is physically dispersed with other cells selected from the group comprising decoupling capacitor cells, electrostatic discharge protection cells and power supply cells.

12. The macro cell of claim 8 wherein the macro cell IO signal slots are dispersed among other, unused IO slots within the macro cell.

13. The macro cell of claim 8 wherein:

the physical layer interface definition further comprises a second clock strobe net electrically coupled to a corresponding one of the macro cell IO slots, wherein signals on the data bus have a desired phase alignment with respect to signals on the second clock strobe net.

14. The macro cell of claim 8 wherein the physical layer interface definition defines circuitry adapted to transfer data over the data bus at a first data rate with every other transition on the first clock strobe net and at a second, faster data rate with each transition on the first clock strobe net.

15. The macro cell of claim 8 wherein:

each bit of the multiple-bit data bus comprises a transmit bit, a receive bit and an enable bit; and

the respective macro cell IO signal slot for each of bit of the data bus defines physical pin locations for the transmit bit, receive bit and enable bit.

16. The macro cell of claim 8 wherein the physical interface definition defines a transceiver configured to implement a PCI-X 2.0 physical layer interface specification.

17. An integrated circuit layout definition comprising:

an input-output (IO) region comprising an interface portion and a plurality of IO buffer cells physically dispersed with other cells in IO slots along the interface portion; and

a macro cell instantiated in the layout definition and comprising:

a plurality of macro cell IO signal slots that are physically dispersed so as to substantially align with corresponding ones of the IO buffer cells in the interface portion;

an interface definition comprising a plurality of source-synchronous interface IO signal nets, which are routed to corresponding ones of the plurality of macro cell signal slots and include a multiple-bit data bus and a clock strobe net, wherein signals on the data bus have a desired phase alignment with respect to signals on the clock strobe net.

18. The integrated circuit of claim 17 wherein the plurality of IO buffer cells is physically dispersed with other cells selected from the group comprising decoupling capacitor cells, electrostatic discharge protection cells and power supply cells.